WHAT IS CLAIMED IS:

1	1. A method of designing an integrated circuit having digital and			
2	analog circuit portions, said digital and analog circuit portions each having defined			
3	functions, comprising:			
4	providing an emulation circuit, which is capable of generating noise;			
5	affixing said emulation circuit on a test substrate;			
6	providing a version of said analog circuit portion having at least some of			
7	said defined functions of said analog circuit portion;			
8	affixing said analog circuit version on said test substrate; and			
9	testing said analog circuit version.			
1	2. The method of claim 1 further comprising modifying said analog			
2	portion in response to said testing step.			
1	3. The method of claim 2 further compromising:			
2	repeating said affixing emulation circuit step, said analog circuit portion			
3	providing step, said analog circuit portion version affixing step and said analog circuit			
4	portion version testing circuit step so that a version of said analog circuit portion having			
5	all of said defined functions of said analog circuit portion, with acceptable response to			
6	said noise effects under operating conditions is obtained.			
1	4. The method of claim 1 further comprising:			
2	providing a version of said digital circuit portion having all of said defined			
3	functions of said digital circuit portion; and			
4	affixing said digital circuit portion version to an integrated circuit			
5	including said version of said analog circuit portion having all of said defined functions of			
6	said analog circuit portion, with acceptable response to said noise effects under operating			
7	conditions.			
1	5. The method of claim 4 wherein said digital circuit portion			
2	providing step includes testing said defined functions of said digital circuit portion			
3	separately from said analog circuit portion.			

1 .		6.	The method of claim 5 wherein said digital circuit portion testing		
2	includes progr	rammin	g an FPGA for testing said defined functions of said digital circuit		
3	portion.				
1		7.	The method of claim 5 wherein said digital circuit portion testing		
2	inaludaa aimu		aid defined functions of said digital circuit portion.		
2	includes siniu	rating s	and defined functions of said digital effects portion.		
1		8.	The method of claim 1 wherein said emulation circuit comprises at		
2	least one array	y compi	rising at least one shift register.		
1		9.	The method of claim 8, wherein said testing said analog circuit		
2	version is perf	formed	while alternately shutting off and turning on at least one array.		
	,				
1		10.	The method of claim 8, wherein said shift register comprises:		
2	•	a plura	ality of flip-flops, each having a clock input for receiving a clock		
3	input signal, and each storing a data bit; and				
4		a plura	ality of interconnecting logic blocks, wherein said plurality of flip-		
5	flops couple to	o each o	other through said plurality of interconnecting logic blocks		
6	sequentially, a	and whe	erein said data bits form a data pattern.		
		1.1	The works defeating 10 whomin gold testing gold analog girquit		
1		11.	The method of claim 10, wherein said testing said analog circuit		
2	version is peri	tormed	while applying a signal at said clock input.		
1	•	12.	The method of claim 11, wherein said testing said analog circuit		
2	version is perf	formed	while varying said clock input signal.		
1		13.	The method of claim 10 wherein said testing said analog circuit		
	version is nort		while varying said data pattern.		
2	version is peri	iomieu	while varying said data pattern.		
1		14.	The method of claim 10, wherein said interconnecting logic blocks		
2	comprise Exc	lusive-C	Or gates, and wherein said testing said analog circuit version is		
3	performed wh	ile vary	ring said data pattern using said Exclusive-Or gates.		
1		15.	The method of claim 10, wherein said interconnecting blocks		
2	comprise a plu	urality o	of logic paths, wherein each logic path is comprised of differing		
3		•	es, and wherein said testing of said analog circuit portion is		
4		-	mately selecting from among said plurality of logic paths.		
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1	16. The method of claim 10, wherein at least one of said flip-flops is		
2	coupled to an equal number of pads through an equal number of output drivers, which		
3	may be enabled and disabled.		
1	17. The method of claim 16, wherein said testing of said analog circuit		
1	,		
2	portion is performed while enabling and disabling said output drivers.		
1	18. The method of claim 1 wherein said analog circuit portion includes		
2	an RF circuit subportion.		
1	19. The method of claim 1, wherein a number of gates in said		
2	emulation circuit is substantially equivalent to a number of gates in said digital circuit		
3	portion.		
1	20. An integrated circuit having digital and analog circuit portions, said		
1			
2	digital circuit portion comprising a digital noise emulation circuit, wherein said digital		
3	noise emulation circuit comprises:		
4	a control block;		
5	at least one array, which comprises at least one shift register; and		
6	a plurality of pads.		
1	21. The integrated circuit of claim 20, wherein each array comprises a		
2	plurality of flip-flops coupled to each other through interconnecting logic blocks.		
1	22. The integrated circuit of claim 21, wherein said flip-flops and		
2	interconnecting logic blocks are coupled sequentially.		
1	23. The integrated circuit of claim 22 wherein said control block		
2	comprises:		
3	a plurality of configuration registers;		
4	at least one input line;		
5	a decoder block for selecting one of said configuration registers for		
6	updating from said at least one input line.		

1	24. The integrated circuit of claim 23, wherein said interconnecting			
2	logic blocks comprise a plurality of logic paths, each path comprising a different amount			
3	of logic gates.			
1	25. The integrated circuit of 24, wherein said plurality of logic paths			
2	are under control of one of said configuration registers.			
1	26. The integrated circuit of claim 23, wherein said interconnecting			
2	logic blocks comprise an Exclusive-Or gate.			
1	27. The integrated circuit of claim 26, wherein said exclusive-or gates			
2	receive at least one input from one of said configuration registers.			
1	28. The integrated circuit of claim 23, wherein at least one flip-flops			
2	couples to an equal number of said plurality of pads.			
1	29. The integrated circuit of claim 28, wherein said at least one flip-			
2	flops couples to an equal number of said plurality of pads though an equal number of			
3	output drivers.			
1	The integrated circuit of claim 29, wherein said output drivers may			
2	be enabled and disabled by one of said configuration registers.			
1	31. A method of designing an integrated circuit having digital and			
2	analog circuit portions, said digital and analog circuit portions each having defined			
3	functions, comprising:			
4	providing an emulation circuit, which is capable of generating noise, and			
5	which comprises a plurality of logic elements;			
6	affixing said emulation circuit on said integrated circuit;			
7	providing a version of said analog circuit portion having at least some of			
8	the defined functions of said analog circuit portion;			
9	affixing said analog circuit version on said integrated circuit;			
10	testing said analog circuit version.			
1	32. The method of claim 31 further comprising modifying said analog			

portion in response to said testing.

1	33. The method of claim 32 further compromising:		
2	repeating said affixing emulation circuit step, said analog circuit portion		
3	providing step, said analog circuit portion version affixing step and said analog circuit		
4	portion version testing circuit step so that a version of said analog circuit portion having		
5	all of said defined functions of said analog circuit portion, with acceptable response to		
6	said noise effects under operating conditions is obtained.		
1	34. The method of claim 31 further comprising reconnecting said logic		
2	elements to provide for said digital portion.		
2	elements to provide for said digital portion.		
1	35. The method of claim 31, wherein said noise generated by said		
2	emulation circuit is substantially equivalent to said digital circuit portion.		
1	36. An integrated circuit having digital and analog portions, designed		
2	by a process comprising:		
3	providing an emulation circuit, which generates noise;		
4	affixing said emulator circuit on a test substrate;		
5	providing a version of said analog circuit portion having at least sone of		
6	said defined functions of said analog circuit portion;		
7	affixing said analog circuit version on said test substrate; and		
8	testing said analog circuit version.		
1	37. The integrated circuit of claim 36, designed by a process further		
2	comprising modifying said analog portion in response to said testing step.		
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1	38. The integrated circuit of claim 37, designed by a process further		
2	compromising:		
3	repeating said affixing emulation circuit step, said analog circuit portion		
4	providing step, said analog circuit portion version affixing step and said analog circuit		
5	portion version testing circuit step so that a version of said analog circuit portion having		
6	all of said defined functions of said analog circuit portion, with acceptable response to		
7	said noise effects under operating conditions is obtained.		
1	39. The integrated circuit of claim 36, designed by a process further		
2	comprising:		
	1		

3	providing a version of said digital circuit portion having all of said defined		
4	functions of said digital circuit portion; and		
5	affixing said digital circuit portion version to an integrated circuit		
6	including said version of said analog circuit portion having all of said defined functions of		
7	said analog circuit portion, with acceptable response to said noise effects under operating		
8	conditions.		
1	40. The integrated circuit of claim 36 wherein said emulation circuit		
2	has at least one array comprising at least one shift register.		
1	41. The integrated circuit of claim 40, wherein said shift register		
2	comprises:		
3	a plurality of flip-flops, each having a clock input for receiving a clock		
4	input signal, and each storing a data bit; and		
5	a plurality of interconnecting logic blocks, wherein said plurality of flip-		
6	flops couple to each other through said plurality of interconnecting logic blocks		
7	sequentially, and wherein said data bits form a data pattern.		
1	42. The integrated circuit of claim 36 wherein said analog circuit		
2	portion includes an RF circuit subportion.		
1	43. The integrated circuit of claim 36, wherein a number of gates in		
2	said emulation circuit is substantially equivalent to a number of gates in said digital		
3	circuit portion.		